AW-CM286NF

IEEE 802.11 1X1 ac/a/b/g/n Wireless LAN + Bluetooth NGFF Module

Datasheet

Version 0.9

Document release	Date	Modification	Initials	Approved
Version 0.1	2016/2/26	Draft version	Peter Chen	Daniel Lee
Version 0.2	2016/3/09	1. 1-4. Specifications Table 2. 1-2. Block Diagram 3. 3-2. High-Speed UART Interface 4. 4. Pin Definition	Peter Chen	Daniel Lee
Version 0.3	2016/4/21	1. 4. Pin Definition 2. 5. Mechanical Information 3. 6. Shipping Information	Peter Chen	Daniel Lee
Version 0.4	2016/8/24	1. 1-4. Specifications Table 2. 4. Pin Definition	Peter Chen	Daniel Lee
Version 0.5	2016/11/1	1. 1-2. Block Diagram 2. 1-3. Key feature 3. 1-4. Specifications Table 4. 2-5. Power up Timing Sequence	Grace Liu	Daniel Lee
Version 0.6	2016/11/8	1. 1-4. Specifications Table	Grace Liu	Daniel Lee
Version 0.7	2017/03/21	Update Block Diagram	Grace Liu	Daniel Lee
Version 0.8	2017/6/8	1. 1-2. Block Diagram 2. 1-3. Key feature 3. 1-4. Specifications Table 4. 3. Host Interfaces 5. 4. Pin Definition	Grace Liu	Daniel Lee
Version 0.9	2017/10/16	Update operation Temperature	Grace Liu	Daniel Lee

1. General Description

1-1. Product Overview and Functional Description

AzureWave Technologies, Inc. introduces the IEEE 802.11ac/a/b/g/n 1X1 WLAN & Bluetooth NGFF module --- **AW-CM286NF**. The module is targeted to mobile devices including **Notebook, TV, Tablet and Gaming Device** which need small package module, low power consumption, multiple interfaces and OS support. By using AW-CM286NF, the customers can easily enable the Wi-Fi, and BT embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11ac/a/b/g/n standard, the AW-CM286NF uses Direct Sequence Spread Spectrum (**DSSS**), Orthogonal Frequency Division Multiplexing (**OFDM**), **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM286NF. In addition to the support of **WPA/WPA2** and **WEP** 64-bit and 128-bit encryption, the AW-CM286NF also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** Wired Equivalent Privacy (**WEP)** with Temporal Key Integrity Protocol (**TKIP)**, Advanced Encryption Standard (**AES**)/Cipher-Based Message Authentication Code (**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms.

For the video, voice and multimedia applications the AW-CM286NF support **802.11e Quality of Service** (**QoS).** The device also supports **802.11h Dynamic Frequency Selection (DFS)** for detecting radar pulses when operating in the 5GHz range.

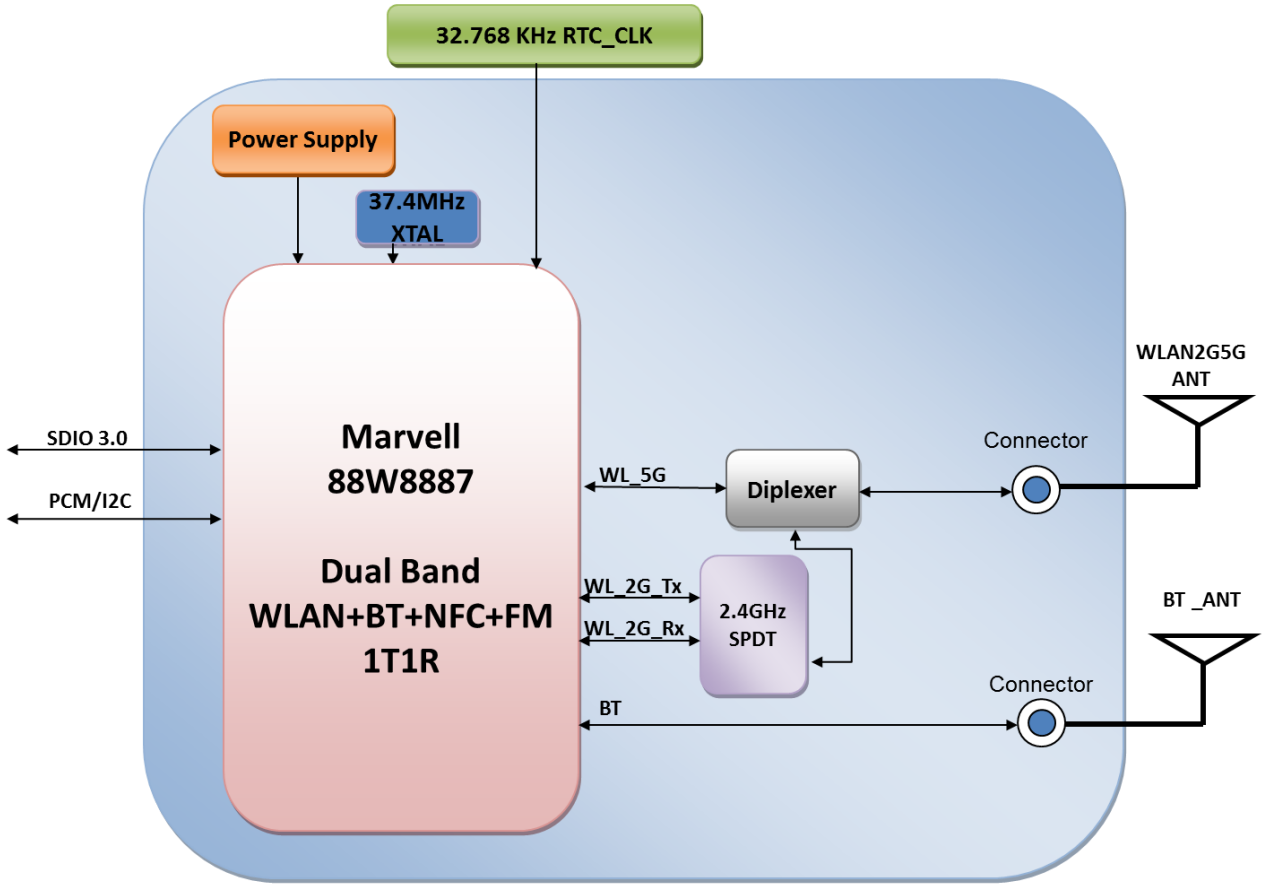
For Bluetooth operation, AW-CM286NF is **Bluetooth 4.2 (supports Low Energy).**

AW-CM286NF supports **SDIO** for WLAN and BT to the host processor.

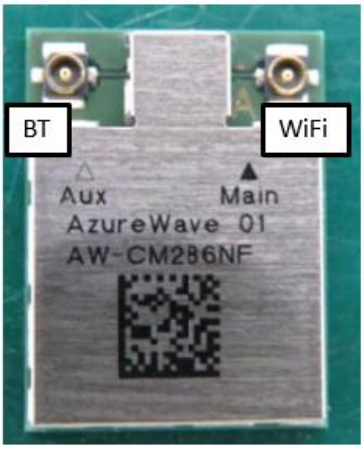
AW-CM286NF module adopts Marvell's latest highly-integrated dual-band WLAN & Bluetooth SoC--- **88W8887**. All the other components are implemented by all means to reach the mechanical specification required.

1-2. Block Diagram

A simplified block diagram of the AW-CM286NF module is depicted in the figure below.



AW-CM286NF BLOCK DIAGRAM



1-3. Key feature:

- **Small footprint: 16mm(L) x 12mm(W) x 1.95mm(H)Max**
- **IEEE 802.11ac compliant, 1x1 spatial stream with data rates up to MCS9 (433 Mbps)**
- **Bluetooth 4.2 (supports Low Energy (LE))**
- **SDIO 3.0 device interface may be used as host interface for WLAN/Bluetooth**
- **PCM/Inter-IC Sound(I2S) for Bluetooth**
- **Audio Codec interface support**
- **Multiple power saving modes for low power consumption**
- **Lead-free design**

1-4. Specifications Table

Model Name	AW-CM286NF
Product Description	**Wireless LAN + Bluetooth Combo Module**
WLAN Standard	IEEE 802.11ac/a/b/g/n, Wi-Fi compliant
Bluetooth Standard	Bluetooth 4.2 complaint with Bluetooth 2.1+Enhanced Data Rate (EDR)
Host Interface	◆ SDIO 3.0 device interface (SPI, 1-bit SDIO, 4-bit SDIO transfer modes at full clock range up to 208 MHz)
Major Chipset	Marvell 88W8887
Dimension	12mm x 16mm x 1.95mm(Max)
Weight	TBD
Package	LGA
Operating Conditions	
Voltage	3.3V+- 10%
Temperature	Operating: -30 ~ 85ºC ; Storage: -40 ~ 85ºC
Electrical Specifications	
Frequency Range	2.4 GHz ISM radio band / 5 GHz Unlicensed National Information Infrastructure (U-NII) band
Number of Channels	802.11a: USA, Taiwan – 12/4 Most European Countries –19 Japan – 4 802.11b: USA, Canada and Taiwan – 11 Most European Countries – 13 France – 4 802.11g: USA, Canada and Taiwan – 11 Most European Countries – 13 Japan – 13 802.11n(HT20): Channel 1~13(2412~2472) 802.11n(HT40): Channel 1~7(2422~2472)
Modulation	DSSS,OFDM,DBPSK,DQPSK,CCK, 16-QAM, 64-QAM 256-QAM for WLAN GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps) for Bluetooth
Output Power	WLAN G band: 11b:16dBm +/- 2dBm(11M) 11g:14dBm +/- 2dBm (54M) 11n HT20:13dBm +/- 2dBm(MCS7) 11n HT40:12dBm +/- 2dBm(MCS7) WLAN A band: 11a:13dBm +/- 2dBm(54M) 11n HT20:12dBm +/- 2dBm(MCS7) 11n HT40:11dBm +/- 2dBm(MCS7) 11ac VHT_20:11dBm +/- 2dBm(MCS8) 11ac VHT_40:10dBm +/- 2dBm(MCS9) 11ac VHT_80: 7dBm +/- 2dBm(MCS9) Bluetooth: Class 2 :2dBm +/- 2dBm

Receive Sensitivity	**WLAN:** **WLAN G band :** **11b:-87dBm (11M)** **11g:-73dBm (54M)** **11n:HT20 -70dBm (MCS7)** **HT40 -68dBm (MCS7)** **WLAN A band:** **11a: -68dBm (54M)** **11n HT20:-66dBm (MCS7)** **11n HT40:-64dBm(MCS7)** **11ac VHT_20: -61dBm(MCS8)** **11ac VHT_40: -58dBm(MCS9)** **11ac VHT_80: -52dBm(MCS9)** **Bluetooth:** **BDR:-88dBm(DH1)** **EDR:-91dBm(2DH5)** **BLE:-94.5dBm**
Data Rates	**WLAN** **802.11b: 1, 2, 5.5, 11Mbps** **802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps** **802.11n: up to 150Mbps** **802.11ac:up to 86.7Mbps (20MHz channel)** **802.11ac:up to 200Mbps (40MHz channel)** **802.11ac:up to 433Mbps (80MHz channel)** **Bluetooth** **Bluetooth 2.1+EDR data rates of 1,2, and 3Mbps**
ESD Rating	**HBM: >2KV per MIL-STD-883H Method 3015.8** **CDM:>500V per JEDEC EIA/JESD22-C101E**
Operating Range	**Open Space: ~300m ; Indoor: ~100m for WLAN** **Minimum 10 m indoor for Bluetooth** **The transmission speed may vary according to the environment)**
Security	◆ **WAPI** ◆ **WEP 64-bit and 128-bit encryption with H/W TKIP processing** ◆ **WPA/WPA2 (Wi-Fi Protected Access)** ◆ **AES-CCMP hardware implementation as part of 802.11i security standard**
Operating System Compatibility	**Linux (Android, Meego), More information please contact Azurewave FAE.**

***WiFi /BT power & sensitivity measure @ module out**

2. Electrical Characteristic

2-1.Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Units
VDD_3V3	3.3V input	--	--	3.3	4.0	V
VIO	Host I/O power supply	--	--	3.3	4.0	V
				2.5	3.0	
				1.8	2.2	
VIO_SD	SDIO power supply	--	--	3.3	4.0	V
				1.8	2.2	

2-2.Recommanded Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VBAT_IN	LDO VBAT input	--	2.7	3.3	3.63	V
VIO	1.8V/2.5V/3.3V digital I/O power supply	--	2.97	3.3	3.63	V
			2.25	2.5	2.75	
			1.62	1.8	1.98	
VIO_SD	1.8V/3.3V digital I/O SDIO power supply	--	2.97	3.3	3.63	V
			1.62	1.8	1.98	

2-3.Clock Specifications

2-3-1 External Sleep Clock Timing

External Sleep Clock is necessary for two reasons:

1. Auto frequency Detection.
   This is where the internal logic will bin the Ref clock source to figure out what is the reference clock frequency is. This is done so no strapping is needed for telling 8887 what the ref clock input is.
2. Allow low current modes for BT to enter sleep modes such as sniff modes.
   The AW-CM286NF external sleep clock pin is powered from the 1.8V voltage supply.

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock Frequency Range	32 or 32.768 -50ppm	32 or 32.768	32 or 32.768 +50ppm	KHz
T_{HIGH}	Clock high time	40	--	--	ns
T_{LOW}	Clock low time	40	--	--	ns
T_{RISE}	Clock rise time	--	--	5	ns
T_{FALL}	Clock fall time	--	--	5	ns

2-4. Reset Configuration

The AW-CM286NF is reset to its default operating state under the following conditions:

- Power-on reset (POR)
- Software/Firmware reset
- External pin reset (RESETn)

2-4-1. Internal Reset

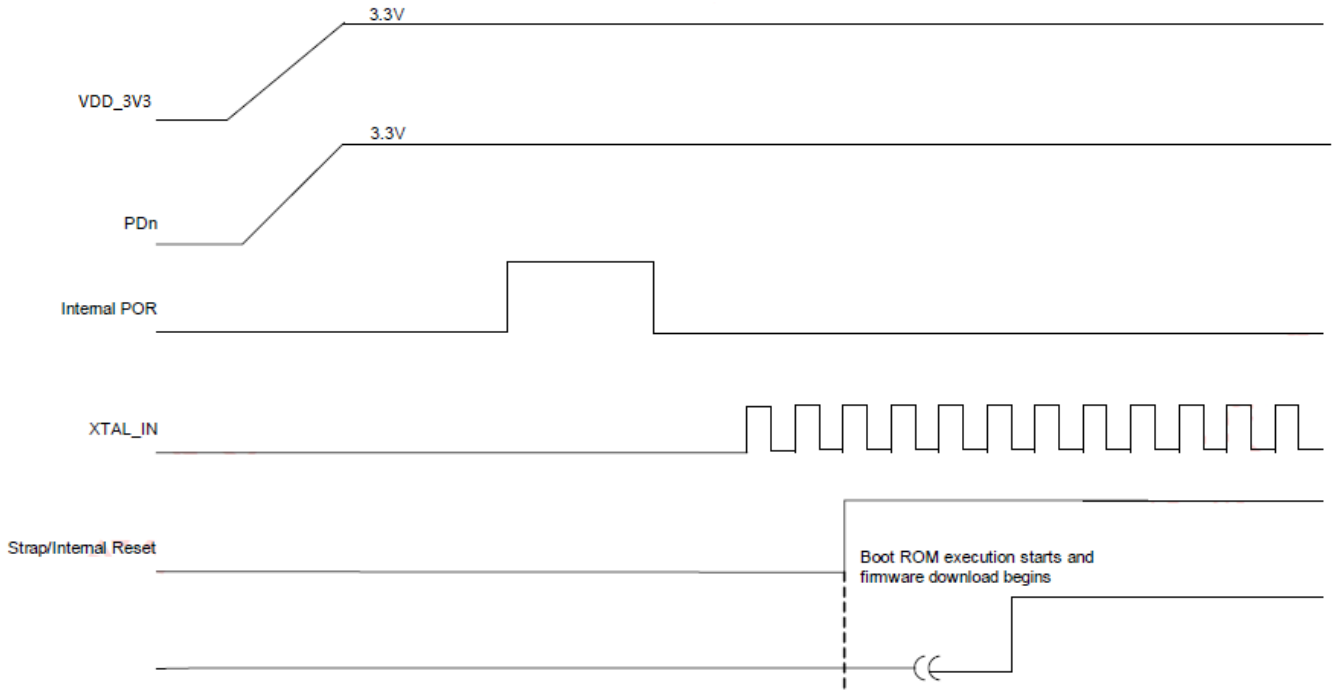
The AW-CM286NF device is reset, and the internal CPU begins the boot sequence when any of the following internal reset events occur:

- Device receives power and VDDL supplies rise (triggers internal POR circuit)
- External pin (PDn) assertion will generate POR

2-4-2. External Reset

The AW-CM286NF is reset when PDn pin is asserted low and the internal CPU begins the boot sequence when the PDn pin transitions from low to high.

2-5. Power up Timing Sequence



3. Host Interfaces

3-1. SDIO Interface

The AW-CM286NF supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless module device.

The AW-CM286NF acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

Supports SDIO 3.0 Standard

On-chip memory used for CIS

Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes

Special interrupt register for information exchange

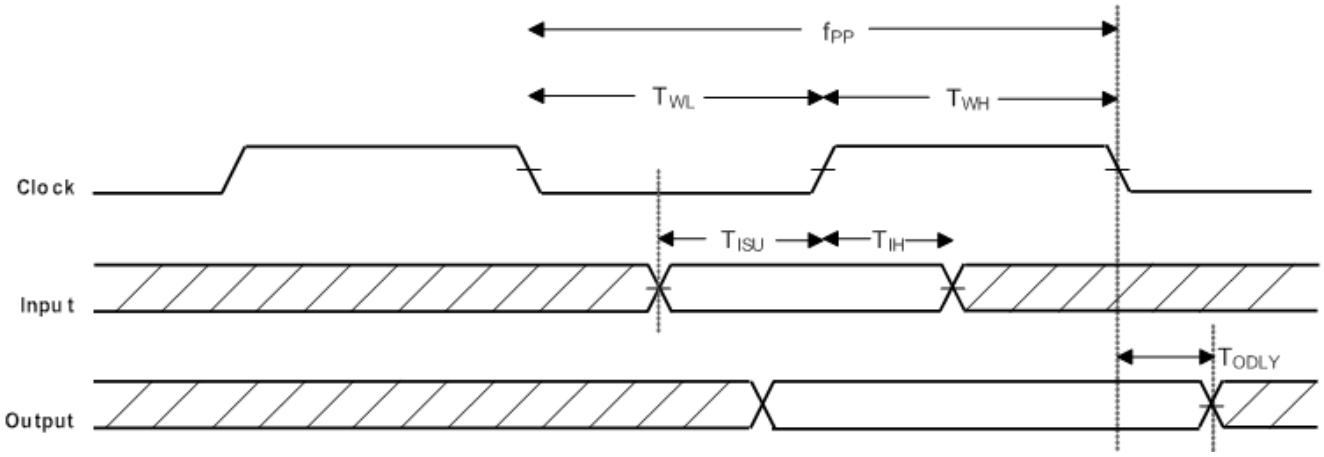
Allows card to interrupt host

3-1-1. SDIO Interface Signal Description

Pin Name	Signal Name	Type	Description
SD_CLK	CLK	I/O	SDIO 1-bit mode: Clock SDIO SPI mode: Clock
SD_CMD	CMD	I/O	SDIO 1-bit mode: Command line SDIO SPI mode: Data input
SD_DAT[3]	DAT3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (active low)
SD_DAT[2]	DAT2	I/O	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPII mode: Reserved
SD_DAT[1]	DAT1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt
SD_DAT[0]	DAT0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data output

3-1-2. Default Speed, High Speed Modes (3.3V)

SDIO Protocol Timing Diagram – Default Speed Mode (3.3V)



SDIO Protocol Timing Diagram – HighSpeed Mode (3.3V)

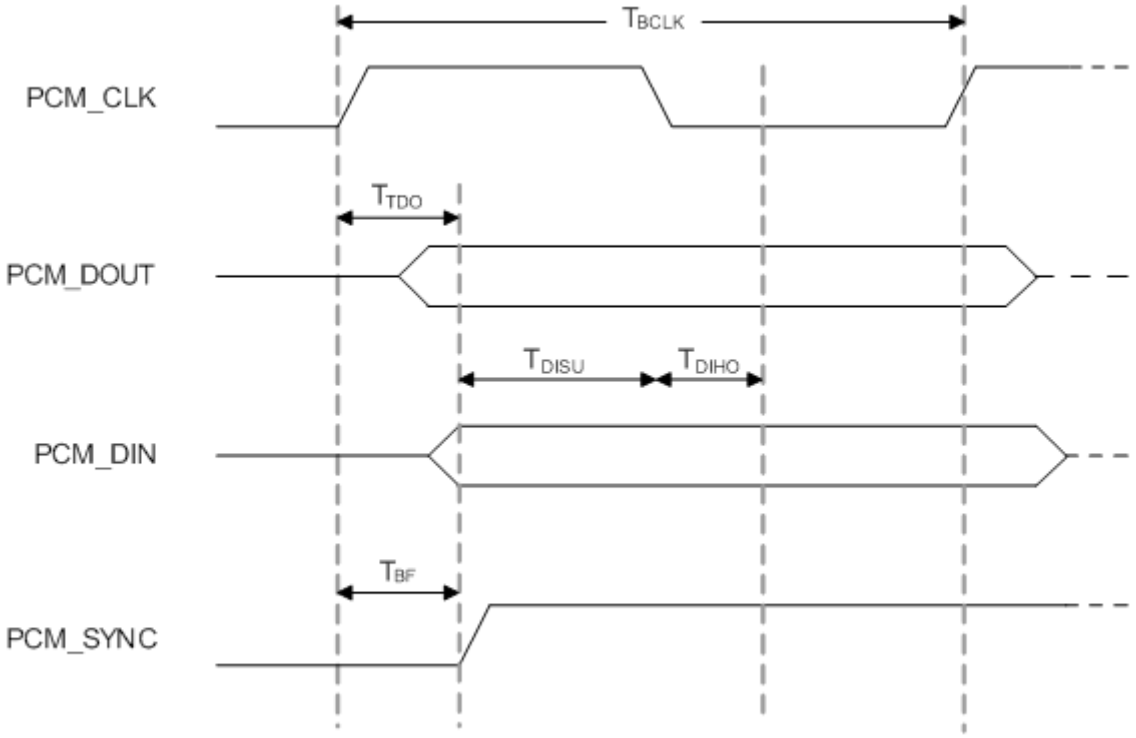
Table shows SDIO Timing Data—Default Speed, High Speed Modes (3.3V)

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency	Default Speed	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WL}	Clock Low Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{WH}	Clock High Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Default Speed	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Default Speed	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time CL ≤ 40 pF (1 card)	Default Speed	--	--	14	ns
		High Speed	---	-1	4	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

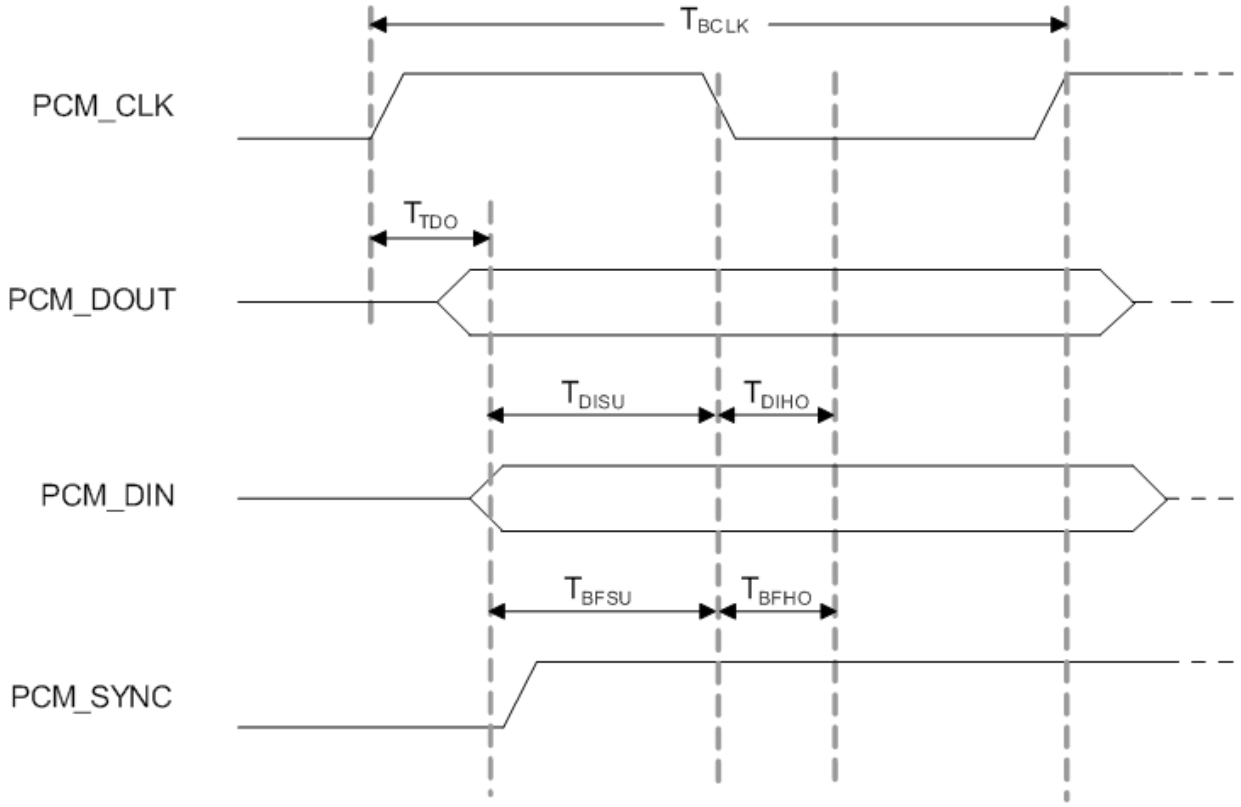
3-2. PCM Interface

3-2-1. PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

3-2-2. PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}	--	--	10	--	--	ns

4. Pin Definition

Pin No	Definition	Basic Description	Type
1	GPIO[15]/TMS	JTAG controller select	
2	GPIO[14]/TCK	JTAG test clock	
3	GPIO[16]/TDI	JTAG test data(input)	I
4	VDD_3V3	3.3V Analog RF Power Supply	I
5	VDD_3V3	3.3V system power supply input	I
6	GND	System Ground Pin	
7	GPIO[17]/TDO	JTAG test data(output)	O
8	NC	No connect	--
9	NC	No connect	--
10	NC	No connect	--
11	GPIO[1]	GPIO[1]	I
12	NC	No connect	--
13	NC	No connect	--
14	NC	No connect	--
15	NC	No connect	--
16	NC	No connect	--
17	GND	System Ground Pin	
18	NC	No connect	--
19	NC	No connect	--
20	GND	System Ground Pin	
21	NC	No connect	--
22	NC	No connect	--
23	GND	System Ground Pin	
24	NC	No connect	--
25	NC	No connect	--
26	GND	System Ground Pin	
27	SLP_CLK	Sleep Clock Input Used for WLAN and Bluetooth low- power modes. External sleep clock of 32.768 KHz must be used for auto reference clock calibration and for WLAN/Bluetooth low power operation.	I

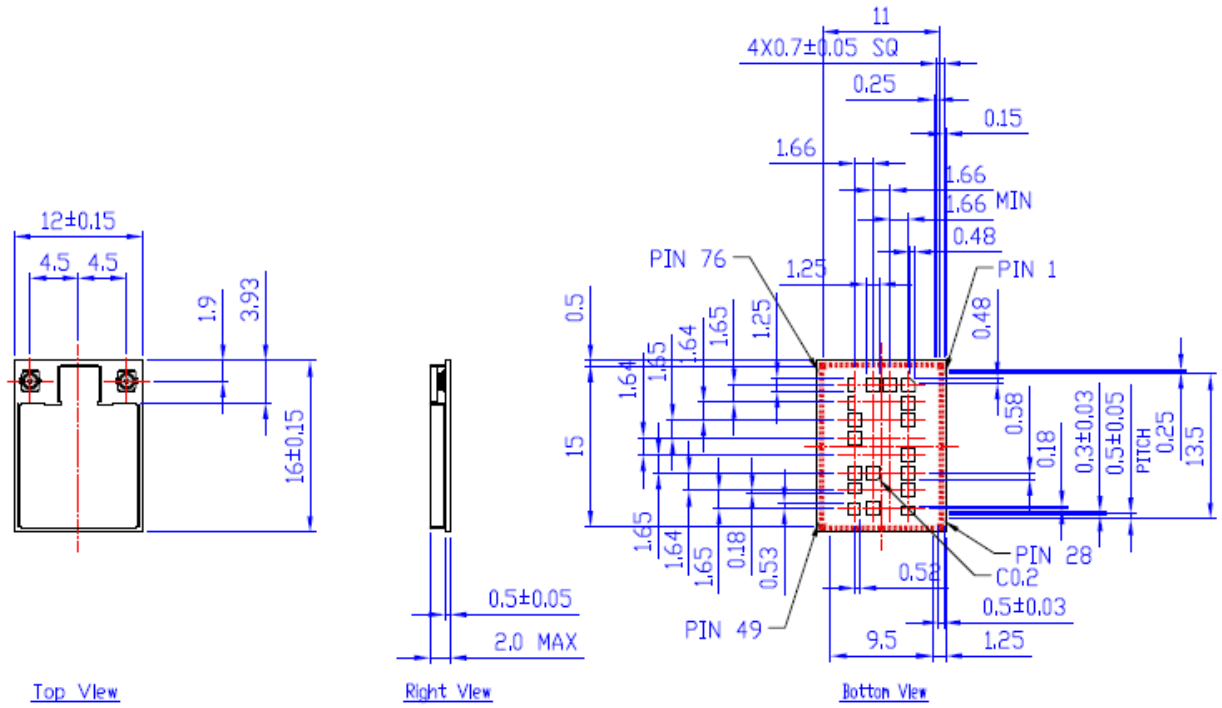
Pin No	Definition	Basic Description	Type
28	GPIO[13]	GPIO[13]	
29	NC	No connect	--
30	NC	No connect	--
31	GPIO[12]	GPIO[12]	--
32	GND	System Ground Pin	
33	NC	No connect	--
34	NC	No connect	--
35	GND	System Ground Pin	
36	NC	No connect	--
37	NC	No connect	--
38	GND	System Ground Pin	
39	NC	No connect	--
40	NC	No connect	--
41	GND	System Ground Pin	
42	GPIO[0]/CLK_REQ	GPIO[0] (input/output)	O
43	NC	No connect	--
44	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply	I
45	PDn	Full Power Down (input) (active low)	I
46	NC	No connect	--
47	SD_DAT[3]	SDIO Data line Bit[3]	I/O
48	SD_DAT[2]	SDIO Data line Bit[2]	I/O
49	SD_DAT[1]	SDIO Data line Bit[1]	I/O
50	SD_DAT[0]	SDIO Data line Bit[0]	I/O
51	SD_CMD	SDIO Command/response (input/output)	I/O
52	SD_CLK	SDIO Clock input	I
53	NC	No Connect	
54	GPIO[10]	GPIO[10] (input/output)	I/O
55	GPIO[8]	GPIO[8] (input/output)	I/O
56	GPIO[9]	GPIO[9] (input/output)	I/O
57	GPIO[11]	GPIO[11] (input/output)	I/O
58	GPIO[7]/PCM_SYNC	GPIO[7] (input/output)	I/O

Pin No	Definition	Basic Description	Type
59	GPIO[4]/PCM_IN	GPIO[4] (input/output)	I
60	GPIO[5]/PCM_OUT	GPIO[5] (input/output)	O
61	GPIO[6]/PCM_CLK	GPIO[6] (input/output)	I/O
62	GND	System Ground Pin	
63	NC	No connect	--
64	GPIO[2]/WLAN_LED	LED_OUT_WLAN (output)	O
65	GPIO[3]/BT_LED	LED_OUT_BT (output)	O
66	NC	No connect	--
67	NC	No connect	--
68	GND	System Ground Pin	
69	NC	No connect	--
70	NC	No connect	--
71	GND	System Ground Pin	
72	NC	No connect	--
73	VIO	Digital I/O Power Supply	I
74	GND	System Ground Pin	
75	GND	System Ground Pin	
76	GND	System Ground Pin	
77	GND	System Ground Pin	
78	GND	System Ground Pin	
79	GND	System Ground Pin	
80	GND	System Ground Pin	
81	GND	System Ground Pin	
82	GND	System Ground Pin	
83	GND	System Ground Pin	
84	GND	System Ground Pin	
85	GND	System Ground Pin	
86	GND	System Ground Pin	
87	GND	System Ground Pin	
88	GND	System Ground Pin	
89	GND	System Ground Pin	

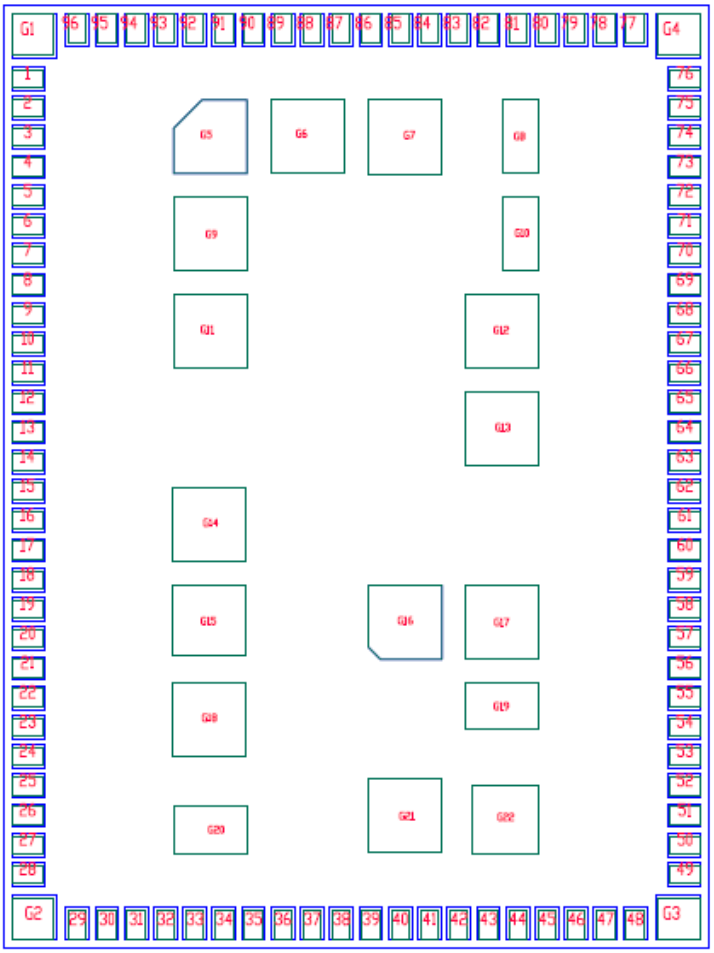
Pin No	Definition	Basic Description	Type
90	GND	System Ground Pin	
91	GND	System Ground Pin	
92	GND	System Ground Pin	
93	GND	System Ground Pin	
94	GND	System Ground Pin	
95	GND	System Ground Pin	
96	GND	System Ground Pin	
G1	GND	System Ground Pin	
G2	GND	System Ground Pin	
G3	GND	System Ground Pin	
G4	GND	System Ground Pin	
G5	GND	System Ground Pin	
G6	GND	System Ground Pin	
G7	GND	System Ground Pin	
G8	GND	System Ground Pin	
G9	GND	System Ground Pin	
G10	GND	System Ground Pin	
G11	GND	System Ground Pin	
G12	GND	System Ground Pin	
G13	GND	System Ground Pin	
G14	GND	System Ground Pin	
G15	GND	System Ground Pin	
G16	GND	System Ground Pin	
G17	GND	System Ground Pin	
G18	GND	System Ground Pin	
G19	GND	System Ground Pin	
G20	GND	System Ground Pin	
G21	GND	System Ground Pin	
G22	GND	System Ground Pin	

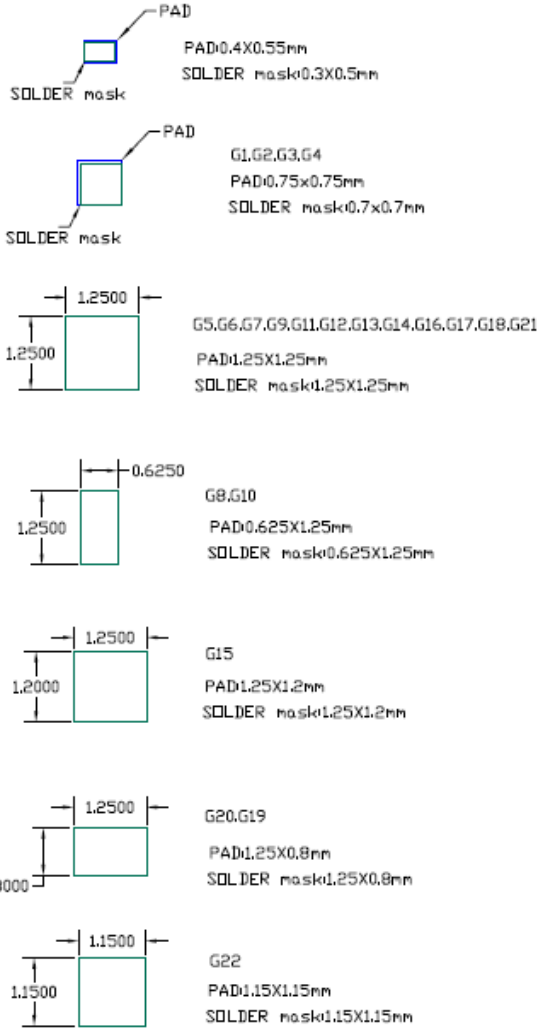
5. Mechanical Information

5-1. Package Outline Drawing



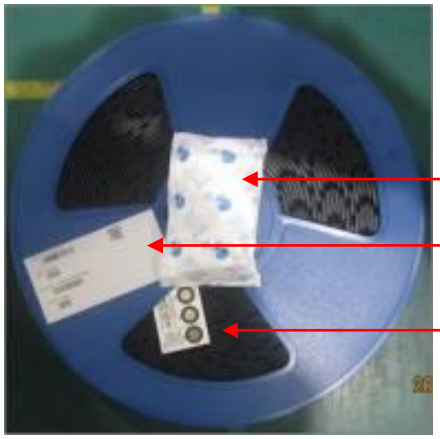
5-2. Module PCB Layout Footprint





6. Shipping Information

6-1



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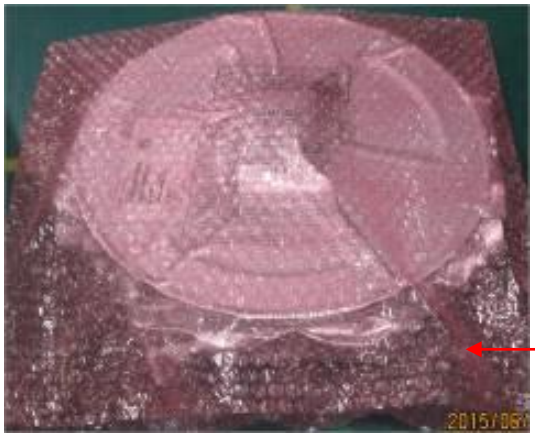
6-3



6-4

6-5

1 Carton= 5 Boxes

6-6

Note: 1 tape reel = 1 box = 1,500pcs

1 carton = 5 boxes = 5 * 1,500pcs=7,500pcs